CLAIMS

What is Claimed is:

1. A method for forming an MIM structure including a protection layer to reduce interdiffusion of an MIM conductive electrode and capacitive dielectric comprising the steps of:

forming a bottom conductive electrode overlying a semiconducting substrate;

forming a first protection layer on the conductive electrode;

forming a dielectric layer on the first protection layer; and,

forming an upper conductive electrode on the dielectric layer to form a metal-insulator-metal (MIM) structure.

2. The method of claim 1, further comprising forming a second protection layer on the dielectric layer prior to the step of forming an upper conductive electrode.

3. The method of claim 2, wherein the second protection layer comprises a silicon rich oxide (SRO) having a relatively higher silicon content compared to stoichiometric SiO_2.

4. The method of claim 1, wherein the first protection layer comprises a silicon rich oxide (SRO) having a relatively higher silicon content compared to stoichiometric SiO_2.

5. The method of claim 1, wherein a portion of the bottom conductive electrode contacting the first protection layer is selected from the group consisting of Ta, TaN, and TaSiN.

6. The method of claim 2, wherein a portion of the upper conductive electrode contacting the second protection layer is selected from the group consisting of Ta, TaN, and TaSiN.

7. The method of claim 1, wherein the dielectric layer comprises PECVD silicon oxide.

8. The method of claim 3, wherein the second protection layer is formed by a PECVD process comprising at least one silicon containing plasma source gas selected from the group consisting of silane (SiH_4), disilane (Si_2H_6), trisilane (Si_3H_8), dichlorosilane (SiH_2Cl_2), trichlorosilane ($SiHCl_3$).

9. The method of claim 8, wherein the second protection layer is formed by a PECVD process comprising a plasma source gas selected from the group consisting of NO and N_2O.

10. The method of claim 4, wherein the first protection layer is formed by a PECVD process comprising at least one silicon containing plasma source gas selected from the group consisting of silane (SiH_4), disilane (Si_2H_6), trisilane (Si_3H_8), dichlorosilane (SiH_2Cl_2), trichlorosilane ($SiHCl_3$).

11. The method of claim 10, wherein the first protection layer is formed by a PECVD process comprising a plasma source gas selected from the group consisting of NO and N_2O.

12. The method of claim 1, wherein the upper and bottom conductive electrodes comprise a metal selected from the group consisting of aluminum, copper, tantalum, tungsten, titanium, and alloys thereof.

13. A method for forming an MIM structure including a protection layer to reduce interdiffusion of an MIM conductive electrode and capacitive dielectric comprising the steps of:

forming a bottom conductive electrode overlying a semiconducting substrate;

forming a dielectric layer on the bottom conductive electrode;

forming a top protection layer on the dielectric layer; and,

forming an upper conductive electrode on the top protection layer to form a metal-insulator-metal (MIM) structure.

14. The method of claim 13, further comprising forming a bottom protection layer on the bottom conductive electrode prior to the step of forming a dielectric layer.

15. The method of claim 13, wherein the top protection layer comprises a silicon rich oxide (SRO) having a relatively higher silicon content compared to stoichiometric SiO_2.

16. The method of claim 14, wherein the bottom protection layer comprises a silicon rich oxide (SRO) having a relatively higher silicon content compared to stoichiometric SiO_2.

17. The method of claim 13, wherein a portion of the upper conductive electrode contacting the top protection layer is selected from the group consisting of Ta, TaN, and TaSiN.

18. The method of claim 14, wherein a portion of the bottom electrode contacting the bottom protection layer is selected from the group consisting of Ta, TaN, and TaSiN.

19. The method of claim 1, wherein the dielectric layer comprises PECVD silicon oxide.

20. The method of claim 13, wherein the top protection layer is formed by a PECVD process comprising at least one silicon containing plasma source gas selected from the group consisting of silane (SiH_4), disilane (Si_2H_6), trisilane (Si_3H_8), dichlorosilane (SiH_2Cl_2), trichlorosilane ($SiHCl_3$).

21. The method of claim 20, wherein the top protection layer is formed by a PECVD process comprising a plasma source gas selected from the group consisting of NO and N_2O.

22. The method of claim 14, wherein the bottom protection layer is formed by a PECVD process comprising at least one silicon containing plasma source gas selected from the group consisting of silane (SiH_4), disilane (Si_2H_6), trisilane (Si_3H_8), dichlorosilane (SiH_2Cl_2), trichlorosilane ($SiHCl_3$).

23. The method of claim 22, wherein the bottom protection layer is formed by a PECVD process comprising a plasma source gas selected from the group consisting of NO and N_2O.

24. The method of claim 13, wherein the upper and bottom conductive electrodes comprise a metal selected from the group consisting of aluminum, copper, tantalum, tungsten, titanium, and alloys thereof.

25. An MIM capacitor structure for use in mixed mode electronic processing comprising:

a bottom conductive electrode;

a first protection layer on the conductive electrode;

a dielectric layer on the first protection layer; and,

an upper conductive electrode on the dielectric layer.

26. The MIM capacitor structure of claim 25, further comprising a second protection layer disposed between the dielectric layer and the upper conductive electrode.

27. The MIM capacitor structure of claim 25, wherein the first protection layer comprises a silicon rich oxide (SRO) having a relatively higher silicon content compared to stoichiometric SiO_2.

28. The MIM capacitor structure of claim 26, wherein the second protection layer comprises a silicon rich oxide (SRO) having a relatively higher silicon content compared to stoichiometric SiO_2.

29. The MIM capacitor structure of claim 25, wherein an uppermost portion of the bottom and upper conductive electrodes comprise a material selected from the group consisting of Ta, TaN, and TaSiN.

30. The MIM capacitor structure of claim 25, wherein the dielectric layer comprises PECVD silicon oxide.

31. The MIM capacitor structure of claim 25, wherein the first protection layer is formed having a thickness between about 25 Angstroms and about 200 Angstroms.

32. The MIM capacitor structure of claim 26, wherein the second protection layer is formed having a thickness between about 25 Angstroms and about 200 Angstroms.

33. The MIM capacitor structure of claim 25, wherein the upper and bottom conductive electrodes comprise a metal selected from the group consisting of aluminum, copper, tantalum, tungsten, titanium, and alloys thereof.

34. An MIM capacitor structure for use in mixed mode electronic processing comprising:

a bottom conductive electrode;

a dielectric layer on the bottom conductive electrode;

a top protection layer on the dielectric layer; and,

an upper conductive electrode on the top protection layer.

35. The MIM capacitor structure of claim 34, further comprising a bottom protection layer disposed between the bottom conductive electrode and the dielectric layer.

36. The MIM capacitor structure of claim 34, wherein the top protection layer comprises a silicon rich oxide (SRO) having a relatively higher silicon content compared to stoichiometric SiO_2.

37. The MIM capacitor structure of claim 35, wherein the bottom protection layer comprises a silicon rich oxide (SRO) having a relatively higher silicon content compared to stoichiometric SiO_2.

38. The MIM capacitor structure of claim 34, wherein an uppermost portion of the upper and bottom conductive electrodes comprise a material selected from the group consisting of Ta, TaN, and TaSiN.

39. The MIM capacitor structure of claim 34, wherein the dielectric layer comprises PECVD silicon oxide.

40. The MIM capacitor structure of claim 34, wherein the top protection layer is formed having a thickness between about 25 Angstroms and about 200 Angstroms.

41. The MIM capacitor structure of claim 35, wherein the bottom protection layer is formed having a thickness between about 25 Angstroms and about 200 Angstroms.

42. The MIM capacitor structure of claim 34, wherein the upper and bottom conductive electrodes comprise a metal selected from the group consisting of aluminum, copper, tantalum, tungsten, titanium, and alloys thereof.